Requirement tracing for design flow in communication protocol IP

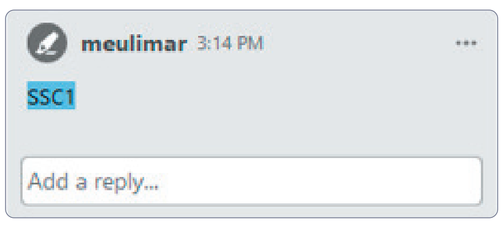
By Marco Meuli from STMicroelectronics
Email: marco.meuli@st.com

The market is requesting different ST products with challenging deadlines. In the Design of System Power Management Interface (SPMI) IP for Analog mixed products, the need to go to market as quickly as possible requires a rigorous methodology. Communication protocol IPs define many features and specific behaviors, and it's quite challenging to keep track of all the details, as well as the bugs that emerge during other phases of the IP flow and slow down overall development. We propose requirements tracing in all the phases of the design, not only at architecture definition level, but also at RTL and verification level.

CORRECTLY TRACED QUALITY DOCUMENTATION SPEEDS UP DEVELOPMENT

1. SPEC: study specification to extract requirements: command codes, features, electrical specs, and timing specification.

The Sequence Start Condition shall be a unique condition on the bus identified by a rising edge followed by a falling edge on SDATA while SCLK remains at a logic low level. The SSC is used by a Slave or Master to identify the start of a Command Sequence.



2. DOS: define architecture that can cover these requirements and add additional requirements that define the behavior of the block.

8.1. SSC Detector
[Covers: SCC1]

[DFE-ID:12251000] Requirement
When the reset signal *i_rst_n* is set to 0, SSC shall not be signaled.
reset value, which is '0.

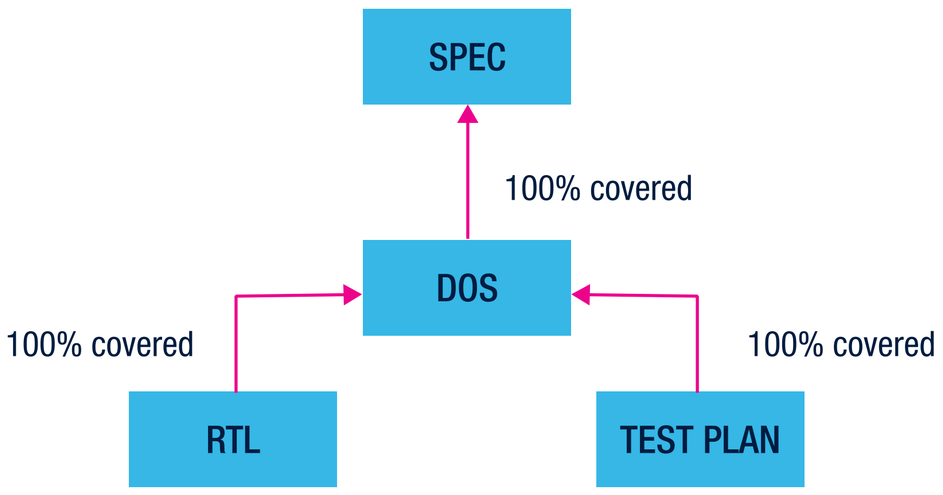
3. TEST PLAN: define a verification plan that simulates and covers the requirements. (each test should cover at least one requirement code).

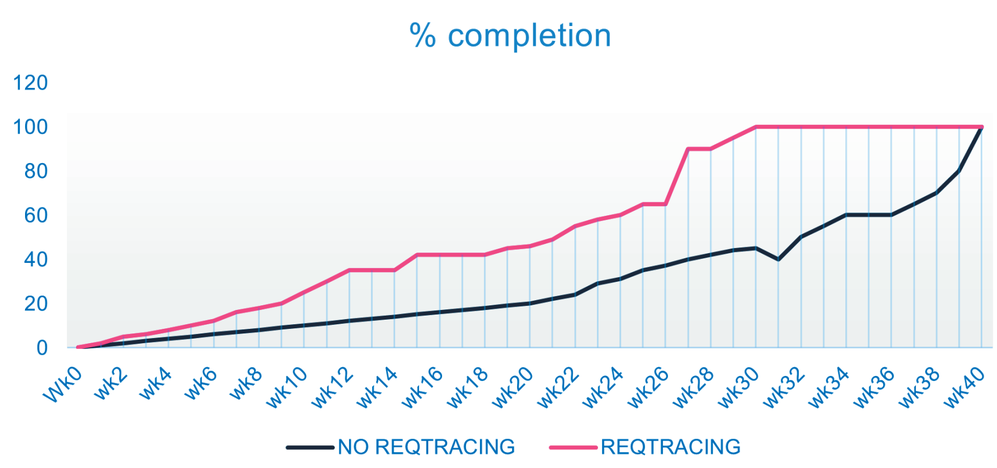
1. SSC			
	ssc pulse detection check	check on the rise of **ssc_pulse_scc** with respect to **i_sdata_rx** when **i_sclk is zero**	[Covers SSC1, DFE-ID:12251000]

4. RTL: write the RTL that specifies which requirements are covered by each part of the code.

```
// [Covers: DFE-ID:12251000]
module spmi_ssc_detector(
```

5. COVERAGE CHECK: instruct the Reqtracer tool to recognize this codes and the connection between one file and another.
Reach 100% requirements covered.





Conclusions

- The need to go to market as quickly as possible requires tackling bugs and missing features at architecture definition level
- Fewer problems propagate into the next phases
- Tracing requirements is vital to speed up the development. Doing so during each phase of the design flow decreases overall delay
- Better design quality reduces bugs encountered during verification by 40%
- Reduced time to market by 20%